REMARKS

Applicants respectfully request reconsideration of the above identified application. Claims 1-30 and 35-46 are pending. Claims 1-30 and 35-46 are rejected.

The Office Communication alleges that Applicant's response filed on January 21, 2005 was not fully responsive to the 35 U.S.C. § 112 first and second paragraph rejections of the Office Action mailed on July 21, 2004. Applicant disagrees, but respectfully offers the following remarks to more fully and effectively respond to the Examiner's rejections under 35 U.S.C. § 112.

Applicant respectfully notes that in the Office Communication mailed on May 31, 2005, remarks with regard to Applicant's arguments of January 21, 2005; interpretations or characterizations by the Examiner, include inferences and/or potential limitations, to which Applicant does not agree.

The remaining comments are directed primarily to the rejected claims.

35 U.S.C. § 112 Rejections

The Office Action mailed on July 21, 2004 rejects Claims 1-30 and 35 under 35 U.S.C. 112, second paragraph, as allegedly failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant respectfully disagrees.

The issue of definiteness is whether, in light of the teachings of the prior art and of the particular invention, the claims set out and circumscribe a particular area with a reasonable degree of precision and particularity. *In re Moore,* 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971).

Claim 1, for example, sets forth:

> 1. (Original) An operating-system transparent method for sharing virtual address translations comprising:
>
> accessing a virtual address translation; and
>
> transparently identifying if the virtual address translation is sharable.

Applicant refers to a definition from McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, (attached) which defines:

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> **transparent** [COMPUT SCI] pertaining to a device or system that processes data without the user being aware of or needing to understand its operation.

Applicant respectfully submits that operating-system transparent is not indefinite, being composed of well known terms of art. Applicant further submits that in light of the prior art and of the particular invention, "transparently identifying if the virtual address translation is sharable," sets out and circumscribes a particular area with a reasonable degree of precision and particularity.

The Office Communication mailed May 31, 2005 states that no attempt was made by Applicant to answer questions brought up by the Examiner's interpretations regarding if and/or how the present disclosure "appeared to define the limitation, 'transparent to the OS.'" In response, Applicant again respectfully submits that the Office Action mailed on July 21, 2004, includes inferences and/or potential limitations, to which Applicant does not agree. The Examiner points to two phrases (one from page 7 and one from page 17) and states that it is not clear whether either or both these definitions must be met.

Applicant respectfully intends that "operating-system transparent" and "transparently identifying if the virtual address translation is sharable," be given the broadest reasonable interpretation consistent with the specification when analyzing the scope of the claim. Applicant respectfully notes: "[t]hat claims are interpreted in light of the specification does not mean that everything in the specification must be read into the claims." *Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 957, 220 USPQ 592, 597 (Fed. Cir. 1983).

In fact, the manner in which the Examiner extracts phrases from the specification while ignoring the context in which they appear is inconsistent with the specification and therefore incorrect when analyzing the scope of the claim. For example the next sentence following the second cited phrase of par. 44 on p. 17 of the specification states, (emphasis supplied)

> "It will also be appreciated that if a multiprocessor or multithreading processor has a mechanism to provide sharing of TLB entries in such a way that is operating-system transparent or operating-system independent, that it does not prohibit that multiprocessor or multithreading processor from also providing for additional operating-system support for managing some sharing of TLB entries."

Therefore the claimed invention does not require all operating systems to be prohibited from supporting or managing sharing of TLB entries as inferred by the Examiner, but rather sets forth at least one operating-system transparent method for transparently identifying if a virtual address translation is sharable.

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Similarly, claim 9 sets forth:

9. (Original) A storage medium having executable codes stored thereon for operating-system transparent sharing of virtual address translations which, when executed by a machine, causes the machine to:
access a virtual address translation; and
transparently identify if the virtual address translation is sharable.

Claim 35 also sets forth:

35. (Original) An operating -system transparent method for providing virtual address translations comprising:
installing an entry in a translation lookaside buffer; and
transparently enabling sharing of the entry by a plurality of processors.

In light of the teachings of the prior art and of the particular invention, claims 1, 9 and 35 clearly set forth operating-system transparent (both being well known terms of art) methods that comprise accessing or installing a virtual address translation and transparently identifying if the virtual address translation is sharable or enabling sharing with a reasonable degree of precision and particularity.

Claim 13 sets forth:

13. (Original) A processing system providing operating-system transparent sharing of virtual address translations, the processing system comprising:
a first logical processor;
a second logical processor;
a storage location to store a virtual address translation; and
a control logic to access a first virtual address translation for the first logical processor in the storage location and to transparently produce a first sharing indication if the virtual address translation may be shared with the second logical processor.

Claim 20 also sets forth:

20. (Original) An apparatus to provide operating-system transparent sharing of virtual address translations, the apparatus comprising:
a control logic to access a first virtual address translation for a first processor,
the control logic further to transparently provide a first sharing indication if the first virtual address translation may be shared with a second processor.

Applicant respectfully submits that in light of the teachings of the prior art and of the particular invention, claims 13 and 20 both set forth apparatus to provide operating-system transparent (both being well known terms of art) sharing of virtual address translations comprising control logic to transparently produce or provide a sharing indication if a virtual address translation may be shared with a reasonable degree of precision and particularity.

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The Office Action mailed on July 21, 2004 also states that it is unclear which operating system is referred to. Applicant respectfully submits that it is not a particular operating system that is being referred to but rather an operating-system transparent method or operating-system transparent sharing of virtual address translations.

The amount of detail required to be included in claims depends on the particular invention and the prior art, and is not to be viewed in the abstract but in conjunction with whether the specification is in compliance with the first paragraph of section 112. *Chemcast Corp. v. Arco Industries Corp.*, 854 F.2d 1328 (Fed. Cir. 1988).

The Office Action mailed on July 21, 2004 also rejects Claims 1-30 and 35 under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. Applicant respectfully disagrees and represents that the specification is in compliance with the first paragraph of § 112.

Applicant also respectfully submits that the Office Action mailed on July 21, 2004 fails to meet the initial burden to establish a reasonable basis to question enablement.

The Examiner says that the present application does not show how to make the identification of sharability of a translation transparent to the operating system, stating that since the PID of Fig. 8 is disclosed as a logical processor, it would not necessarily be generated by hardware and may be set by the process or some other software mechanism. The Examiner then concludes that the disclosure has not shown how to prevent a requirement to modify the operating system to set and submit the PID.

According to MPEP § 2164.04, before any analysis of enablement can occur, it is necessary for the Examiner to construe the claim. As stated above with regard to the second paragraph of § 112, the manner in which the Examiner extracts phrases from the specification while ignoring the context in which they appear is inconsistent with the specification and therefore incorrect when analyzing the scope of the claim. Thus, by construing the claim in a manner inconsistent with the specification, the Examiner concludes that the specification does not enable the claim.

Applicant respectively submits that the Examiner can make no prima facie case for lack of enablement by improperly construing the claims to be inconsistent with the specification. Applicant therefore respectfully requests the Examiner withdraw rejection of claims 1-30 and 35

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under 35 U.S.C. 112, first paragraph, for failing to meet the initial burden to establish a reasonable basis to question enablement.

Therefore, Applicant believes that the Office Action rejections of claims 1-30 and 35 under 35 U.S.C. 112, first paragraph, have been responded to fully and that no additional remarks are necessary. Never-the-less, Applicant would like take the opportunity to fully address the Examiner's allegations of non-responsiveness to the Office Action mailed July 21, 2004.

The claimed invention does not require operating systems to be prevented from setting and submitting a PID as inferred by the Examiner, but rather sets forth at least one operating-system transparent method for transparently identifying if a virtual address translation is sharable.

The Examiner refers to the cited 102(e) reference, U.S. Patent 6,598,050 B1 (Bourekas), as a "seemingly similar translation sharing implementation," and as having "an equivalent process identifier." Applicant respectfully submits that the point lies not in broad and over-simplified characterizations, but rather in whether the cited reference discloses some operating-system transparent method for transparently identifying if a virtual address translation is sharable. As Applicant has respectfully asserted in previous communications, Bourekas does not.

The Examiner has also pointed out that how the PID is generated is apparently not disclosed. The specification need not disclose what is well-known in the art and preferably omits that which is well-known to those skilled and already available to the public. *In re Buchkner,* 929 F.2d 660, 661, 18 USPQ2d 1331, 1332, (Fed. Cir. 1991).

For example, the specification discloses that (p. 14-16, par. 37-40, emphasis supplied):

> A variation of multiprocessing is known in the art as multithreading. In multithreading, multiple logical processors, which may comprise a single physical processor or multiple physical processors, perform tasks concurrently.

Applicant also refers the Examiner to an article submitted in an accompanying IDS, "On the Performance of A Multi-Threaded RISC Architecture," by Scott Lindsay and Bruno Preiss, of September 1993, p. 5, lines 42-43, which indicates that thread identifiers in multithreading processors were well-known in the art prior to the time of filing the present application.

Applicant respectfully intends that in light of the prior art and of the present specification, for example with regard to Figures 7b and 8, one of skill in the art would be able to generate a PID for a logical processor without undo experimentation.

Applicant also respectfully submits that, with regard to transparently identifying if the virtual address translation is sharable, the specification has set forth a full and clear description of

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the claimed subject matter in sufficient detail to support a conclusion by one skilled in the art that Applicant had possession of the claimed invention and further, to enable one skilled in the art to make and use the claimed invention. For example, the specification discloses (p. 14-16, par. 37-40, emphasis supplied):

> Control logic 604 may use the data portion 614, sharing indication 619, and data portion 624 to identify if the virtual address translation is sharable. For example, if a processor initiates a TLB request to look up a virtual address translation and the TLB entry in latches 633 and 637 contains an ASID that matches the ASID for the virtual address to be translated, and further if the entry contains a VAD that matches the VAD for the virtual address, and finally if sharing indication 619 indicates a set of logical processes including one associated with the processor initiating the TLB request, then the entry in latch 633 and latch 637 may be used to translate the virtual address. Otherwise, control logic 604 may initiate installation of a new virtual address translation entry for TLB 602.
>
> Whenever a miss occurs in TLB 602, the physical address data and other TLB data may be recovered from page tables in main memory. For one alternative embodiment control logic 604 may comprise a mechanism for recovering such data. Most modern processors use a mechanism called a page walker to access page tables in memory and compute physical addresses on TLB misses.
>
> If a processor, either directly through software or indirectly through control logic 604, initiates a TLB request to installation of a new virtual address translation entry, the TLB 602 may be searched for any existing entries that can be shared. An entry retrieved from tag array 631 and translation array 635 may then be latched by latch 633 and latch 637 respectively. If the TLB entry in latches 633 and 637 contains an ASID that matches the ASID for the virtual address to be translated, and further if the entry contains a VAD that matches the VAD for the virtual address, and finally if sharing indication 619 indicates a shared status, then the entry in latch 633 and latch 637 may be installed for the processor initiating the TLB request by adding the logical process associated with the initiating processor to the set of logical processes indicated by sharing indication 619 and thereafter the TLB entry may be used to translate the virtual address. Otherwise, control logic 604 may initiate allocation of a new virtual address translation entry for TLB 602.
>
> If a processor, either directly through software or indirectly through control logic 604, initiates a TLB request to allocate a new virtual address translation entry, the TLB 602 may be searched for any invalid or replaceable entries. The retrieved TLB entry may then be reset by control logic 604 to contain an ASID that matches the ASID for the virtual address to be translated, a VAD that matches the VAD for the virtual address, a PAD that matches the PAD of the translated physical address, an ATRD that matches the ATRD of the translated physical address, and any other associated data corresponding to the virtual address translation. Finally the entry may be installed for the processor initiating the TLB allocation request by initializing the set of logical processes indicated by sharing indication 619 to contain only the logical process associated with the initiating processor. It will be appreciated that the sharing indication 619 may be conveniently initialized by default to indicate a shared status for the virtual address translation. Alternatively if the allocation was initiated through software, for example, control logic 604 may initialize the sharing indication 619 by default to indicate a private status for the virtual address translation.

Therefore, Applicant respectfully intends that one of skill in the art would be able to transparently identify if the virtual address translation is sharable without undo experimentation. The present specification further states with regard to Fig. 7a (p. 19, par. 46-48, emphasis supplied):

> In Figure 7a, for example, a sharing indication corresponding to virtual address translation entry 711 indicates a private status of P and a set of logical processes of 0001, the low order bit being set to indicate that entry 711 may be used exclusively to translate virtual addresses for processor 710. Similarly a sharing indication corresponding to virtual address translation entry 713 indicates a private status of P and a set of logical processes of 0100, indicating that entry 713 may be used exclusively to translate virtual addresses for processor 740.

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A sharing indication corresponding to virtual address translation entry 712 indicates a shared status of S and a set of logical processes of 0101, indicating that entry 712 may be shared and may be used to translate virtual addresses for processors 710 and 740. Similarly a sharing indication corresponding to virtual address translation entry 719 indicates a shared status of S and a set of logical processes of 1111, indicating that entry 719 may be shared and used to translate virtual addresses for all four processors 710-780.

A sharing indication corresponding to virtual address translation entry 716 indicates a invalid status of I and a set of logical processes of 0000 meaning that entry 716 may not be used to translate virtual addresses for any processor 710-780. It will be appreciated that the invalid status may be explicitly represented or implicitly represented by the corresponding set of logical processes. It will also be appreciated that one skilled in the art may produce other encodings to explicitly or implicitly represent sharing indications for TLB entries.

The specification further states with regard to Fig. 7b (p. 20, par. 49-50, emphasis supplied):

In Figure 7b, for example, a sharing indication corresponding to virtual address translation entry 711 may implicitly indicate a private status of P and an explicit set of logical processes of 01 meaning that entry 711 may be used to translate virtual addresses for processor 710. It will be appreciated that such an implicit status representation may permit any implicit private status to be changed to an implicit shared status if another processor is found that may make use of the corresponding virtual address translation entry.

For example, if a processor initiates a TLB request to look up a virtual address translation and the sharing indication corresponding to the retrieved TLB entry indicates a set of logical processes that does not include one associated with the processor initiating the TLB request, then the physical address data and other TLB data may be recovered from page tables in main memory. Control logic 704 may include a mechanism for recovering such data, or may invoke a mechanism such as a page walker to access page tables in memory and compute physical addresses. If the newly constructed virtual address translation matches the retrieved TLB entry, the requesting process may be added to the set of logical processes sharing the retrieved TLB entry. Otherwise the newly constructed virtual address translation may be installed in a new TLB entry for the requesting processor.

Therefore, Applicant respectfully submits that the present application discloses how to make the identification of sharability of a translation transparent to the operating system such that one skilled in the art may practice the entire scope of the subject matter claimed without undo experimentation. Therefore, Applicant respectfully requests the Examiner withdraw his rejections under 35 U.S.C. 112, first and second paragraphs.

CONCLUSION

Applicants respectfully submit the present claims for allowance.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

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If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence Mennemeier at (408) 765-2194.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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range just above and just below the acoustic velocity. tran'sän·ik 'flō }

nsonic range [FL MECH] The range of speeds between speed at which one point on a body reaches supersonic eed, and the speed at which all points reach supersonic speed. tran'sän·ik 'rānj }

nsonic speed [FL MECH] The speed of a body relative the surrounding fluid at which the flow is in some places the body subsonic and in other places supersonic. tran'sän·ik 'spēd }

nsonic wind tunnel [ENG] A type of high-speed wind nnel capable of testing the effects of airflow past an object speeds near the speed of sound, Mach 0.7 to 1.4; sonic speed ccurs where the cross section of the tunnel is at a minimum, at is, where the test object is located. { tran'sän·ik 'wind ən·əl }

nsorbital lobotomy [MED] A lobotomy performed rough the roof of the orbit. { tranz'ȯr·bəd·əl lə'bäd·ə·mē }

nsosonde [ENG] The flight of a constant-level balloon, hose trajectory is determined by tracking with radio-direction-nding equipment; thus, it is a form of upper-air, quasi-horizontal sounding. { 'tran·zə,sänd }

nsparency [GRAPHICS] An image fixed on a clear base by eans of a photographic, printing, chemical, or other process, pecially adaptable for viewing by transmitted light. PTICS] The ability of a substance to transmit light of differ-t wavelengths, sometimes measured in percent of radiation hich penetrates a distance of 1 meter. { tranz'par·ən·sē }

nsparency range [NUC PHYS] A postulated energy range r extremely high-energy heavy-ion collisions in which the ojectile passes through the target and emerges with its temper-ure and density raised to the point at which a quark-gluon sma forms. { tranz'par·ən·sē ,rānj }

nsparent [COMPUT SCI] Pertaining to a device or system at processes data without the user being aware of or needing understand its operation. [PHYS] Permitting passage of diation or particles. { tranz'par·ənt }

nsparent medium [OPTICS] 1. A medium which has the operty of transmitting rays of light in such a way that the uman eye may see through the medium distinctly. 2. A edium transparent to other regions of the electromagnetic ectrum, such as x-rays and microwaves. { tranz'par·ənt əd·ē·əm }

nsparent sky cover [METEOROL] In United States eather-observing practice, that portion of sky cover through hich higher clouds and blue sky may be observed; opposed opaque sky cover. { tranz'par·ənt 'skī ,kəv·ər }

nspassive region [PHYS CHEM] That portion of an odic polarization curve in which metal dissolution increases the potential becomes noble. { tranz'pas·iv ,rē·jən }

nsphasor [OPTICS] A nonlinear optical device that uses light beam to modulate another, in a manner analogous to electronic transistor, and that operates through the transfer-ce of a phase shift from one beam to the other. { ,tranz ,fāz·ər }

nspiration [BIOL] The passage of a gas or liquid (in the form of vapor) through the skin, a membrane, or other tissue. ,tranz·pə'rā·shən }

nspiration cooling *See* sweat cooling. { ,tranz·pə'rā·shən ,kül·iŋ }

nsplantation [BIOL] 1. The artificial removal of part of n organism and its replacement in the body of the same or of a different individual. 2. To remove a plant from one location nd replant it in another place. { ,tranz·plan'tā·shən }

nsplantation antigen [IMMUNOL] An antigen in a cell which induces a histocompatibility reaction when the cell is transplanted into an organism not having that antigen. ,tranz·plan'tā·shən 'ant·i·jən }

nsplantation disease [MED] Disease ascribable to an immunological graft-versus-host reaction which occurs after transplantation of adult lymphoid cells to incompatible recipients who cannot reject them. { ,tranz·plan'tā·shən di,zēz }

nsplanter [AGR] A special kind of equipment designed for the planting of cuttings or small plants; it transports one or more workers who assist the action of the machine in placing plants in a furrow and covering them; it commonly supplies a small quantity of water to each plant. { tranz'plan·tər }

nsplutonium element [INORG CHEM] An element having an atomic number greater than that of plutonium (94). { ,tranz·plə'tō·nē·əm 'el·ə·mənt }

transpolarizer [ELEC] An electrostatically controlled circuit impedance that can have about 30 discrete and reproducible impedance values: two capacitors, each having a crystalline ferroelectric dielectric with a nearly rectangular hysteresis loop, are connected in series and act as a single low impedance to an alternating-current sensing signal when both capacitors are polarized in the same direction; application of 1-microsecond pulses of appropriate polarity increases the impedance in steps. { tranz'pō·lə,rīz·ər }

transponder [COMMUN] 1. A transmitter-receiver capable of accepting the challenge of an interrogator and automatically transmitting an appropriate reply. 2. A receiver-transmitter, such as on satellites, which receives a transmission and retransmits it at another radio frequency. { tranz'pän·dər }

transponder beacon *See* responder beacon. { tranz'pän·dər ,bē·kən }

transponder dead time [ELECTR] Time interval between the start of a pulse and the earliest instant at which a new pulse can be received or produced by a transponder. { tranz'pän·dər 'ded ,tīm }

transponder set [ELECTR] A complete electronic set which is designed to receive an interrogation signal, and which retransmits coded signals that can be interpreted by the interrogating station; it may also utilize the received signal for actuation of additional equipment such as local indicators or servo amplifiers. { tranz'pän·dər ,set }

transponder suppressed time delay [ELECTR] Overall fixed time delay between reception of an interrogation and transmission of a reply to this interrogation. { tranz'pän·dər sə'prest 'tīm di,lā }

transport [COMPUT SCI] 1. To convey as a whole from one storage device to another in a digital computer. 2. *See* tape transport. [ENG] Conveyance equipment such as vehicular transport, hydraulic transport, and conveyor-belt setups. [NAV ARCH] A ship designed to carry military personnel from one place to another. Also known as troop ship. { trans'pȯrt (verb), 'tranz,pȯrt (noun) }

transportable computer [COMPUT SCI] A microcomputer that can be carried about conveniently but, in contrast to a portable computer, requires an external power source. { tran·z'pȯrd·ə·bəl kəm'pyüd·ər }

transportation [GEOL] A phase of sedimentation concerned with movement by natural agents of sediment or any loose or weathered material from one place to another. { ,tranz·pər'tā·shən }

transportation emergency [ENG] A situation which is created by a shortage of normal transportation capability and of a magnitude sufficient to frustrate movement requirements, and which requires extraordinary action by the designated authority to ensure continued movement. { ,tranz·pər'tā·shən i,mər·jən·sē }

transportation engineering [ENG] That branch of engineering relating to the movement of goods and people; major types of transportation are highway, water, rail, subway, air, and pipeline. { ,tranz·pər'tā·shən ,en·jə,nir·iŋ }

transportation lag *See* distance/velocity lag. { ,tranz·pər'tā·shən ,lag }

transportation priorities [ENG] Indicators assigned to eligible traffic which establish its movement precedence; appropriate priority systems apply to the movement of traffic by sea and air. { ,tranz·pər'tā·shən prī,är·əd·ēz }

transportation problem [IND ENG] A programming problem that is concerned with the optimal pattern of the distribution of goods from several points of origin to several different destinations, with the specified requirements at each destination. { ,tranz·pər'tā·shən ,präb·ləm }

transport capacity [ENG] The number of persons or the tonnage (or volume) of equipment which can be carried by a vehicle under given conditions. { 'tranz,pȯrt kə,pas·əd·ē }

transport case [ENG] A moistureproof nonconductive wood, plastic, or fabric container used to transport safely small quantities of dynamite sticks to and from blasting sites. { 'tranz,pȯrt ,kās }

transport cross section [PHYS] The product of the total scattering cross section and the average value of $1 - \cos\theta$, where θ is the laboratory scattering angle. { ,tranz,pȯrt 'krȯs ,sek·shən }

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